REMARKS

Attached hereto is an Excess Claims Letter and fee.

It is noted that the claim amendments above are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-31 are all of the claims pending in the present Application. New claims 26-31 have been added.

Claim 7 stands rejected under 35 USC §112, second paragraph, as being indefinite. Claims 1 and 4 stand rejected under 35 USC §102(b) as anticipated by US Patent 5,177,593 to Abe. Claims 3 and 5-21 stand rejected under 35 USC §103(a) as unpatentable over Abe. Claims 22-25 stand rejected under 35 USC §103(a) as unpatentable over Abe, further in view of US Patent 6,093,940 to Ishinaga et al.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example, by claim 1, the present invention is directed to a light emitting device including an insulating base having a plurality of electrical leads including positive and negative leads provided on top and bottom surfaces thereof. A common (continuous) metal layer makes up each of a negative lead on the top surface and a negative lead on the bottom surface. An LED chip array is arranged on the negative lead on

the top surface of the insulating base. The LED chip array is electrically connected to the positive and negative leads on the top surface of the insulating base. A plurality of first metal connections is configured to respectively interconnect the positive leads on the top and bottom surfaces of the insulating base. At least one second metal connection is configured to interconnect the negative leads on the top and bottom surfaces of the insulating base. For each of the at least one second metal connection, one LED chip of said LED chip array is mounted directly thereon.

The present invention provides a light emitting device in which homogeneous radiation characteristics is obtained and, thereby, provides the advantages that no significant change in color balance occurs over time and longer service life.

II. THE 35 USC §112, SECOND PARAGRAPH, REJECTION

Claim 7 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner considers that an LED device in which inherently a single voltage level is distributed would have equal heat amounts for each LED chip mounted therein.

Applicants submit that the Examiner's confusion is perhaps due to failing to realize that each LED chip configuration would have a unique I-V diode characteristic. Therefore, assuming a same voltage to each chip, the resultant current will vary for each LED type according to its diode characteristic. As explained in the specification in paragraph [0051], relative to the red LED type, the green and blue LEDs consume considerably more current, thereby dissipating considerable more heat.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTION

The Examiner alleges that Abe anticipates the present invention as defined by claims 1 and 4. Applicants respectfully disagree.

First, relative to claim 1, a key feature of the present invention is that the heat dissipation of the various LED chips is equalized. Accordingly, all the LED chips are mounted on a common metal layer on the top surface of the base. As shown in Figure 4A, Abe clearly fails to teach or suggest this feature and, indeed, teaches against it.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of " ...a negative lead on said top surface and a negative lead on said bottom surface each comprising a common metal layer...."

Even assuming *arguendo* that Ishinaga teaches a single metal layer 4 upon which the LED chips 2a, 2b are mounted, Ishinaga fails to teach or suggest that the heat dissipation is critical. Accordingly, in Ishinaga, there is no teaching or suggestion to reduce the length of the heat dissipation path to the lower metal layer by forming the metal interconnections as being directly below the LED chips having the highest heat dissipation. Indeed, the location of interconnection 5 in Ishinaga teaches against this feature of the present invention.

Hence, in Ishinaga, there is no teaching or suggestion of " ... at least one LED chip of said LED chip array is mounted directly on each said at least one second metal connection".

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Relative to the rejection for claims 3 and 5-21, the Examiner is understood as considering that the components and arrangements of the prearranged array of blue, green, and red LED chips are well known in the art to produce white light. However, since the

Examiner is understood as taking Office Notice, Applicants request that a reasonable citation properly combinable with the other applied references be provided for the specific configurations described in these claims, including the ordering and the quantities as described.

Relative to the rejection beginning at the bottom of page 4 of the Office Action and labeled as "2", Applicants request that the Examiner clarify which claim(s) is being rejected, particularly since neither Abe nor Ishinaga teach or suggest an LED array in which the heat dissipation is discussed, as described in claims 7 and 21, or that the wire bonding is arranged to be on one side, as described in claims 10-12, or that the through-hole interconnects be located beneath the LED chips, as described in claim 17.

Relative to the rejection for claims 13 and 14 on page 6 of the Office Action, the Examiner seems confused in failing to provide patentable weight to the limitations describing method steps. These claims are product-by-process claims, as described in MPEP §2113 and MPEP §2173.05(p), and are clearly proper, as indicated by the first sentence in the latter section, as follows: "*A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper.*"

As per the guideline in MPEP §2113, the Examiner has the initial burden of identifying a same or similar product, even if produced by a different process. Only then does the burden shift to Applicant.

Relative to the rejection for claims 22-25, the Examiner is understood as conceding that Abe fails to teach a common metal layer upon which a plurality of LED chips are mounted. The Examiner relies upon Ishinaga to overcome this deficiency. In urging this combination, the Examiner alleges:

"*It would have been obvious to one of ordinary skill in the art at the time the*

invention was made to modify the LED device of Abe with the LED device of Ishinaga et al since as taught by Ishinaga the improvements of the connections and materials used in the LED chip display are useful for the purpose of providing a more suitable connection array for LED chip displays."

Applicants respectfully disagree that the above combination is proper as meeting the burden of a prima facie rejection under 35 USC § 103(a).

First, this rejection is improper under the guideline of MPEP §2143.02: "*The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination* (Emphasis in MPEP)."

Second, this rejection is improper under the guideline of MPEP §2143.02: "*If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.*" More specifically, Ishinaga teaches mounting the LED carrier 101 on its side. Such arrangement would totally defeat the purpose of the alpha-numeric display of Abe, in which the observer must be able to discern which specific LED segments are being activated.

Moreover, even if Abe and Ishinaga would have been combined as urged by the Examiner, the combination would still fail to result in the invention as defined by these claims. Specifically, in one aspect, the present invention addresses a problem in the art in which heat dissipation causes a degradation in performance. The solution of the present invention includes positioning the LED chips as based on heat dissipation (e.g., claim 21) and locating the metal interconnects directly below the critical LED chip or chips (e.g., claim 23). Neither Abe nor Ishinaga teach or suggest a structure based on relative heat dissipation.

For the reasons stated above, the claimed invention is fully patentable over the cited

references.

Further, the other prior art of record has been reviewed, but it too, even in combination with Abe or Ishinaga, fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-31, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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Frederick E. Cooperrider
Reg. No. 36,769

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254